ABSTRACT

A clock shrink circuit has an inverting first matching stage which is responsive to an input clock signal to generate a first inverted signal having a first matching delay. The first matching delay is a difference between a first rise and a first fall propagation time of the first matching stage. An inverting first pull-up stage is coupled to the first matching stage and is responsive to the first inverted signal to generate a second inverted signal having a first pull-up delay which is substantially reduced by the first matching delay. The first pull-up delay is a difference between a second rise and a second fall propagation time of the first pull-up stage.